



AMERICAN INTERNATIONAL UNIVERSITY-BANGLADESH (AIUB)
Faculty of Engineering
Department of EEE and CoE Undergraduate Program

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Ex: 08

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Title : Construction of MOSFET Logic Gates (Part I)

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Faculty of Engineering

Department of EEE

American International University-Bangladesh

Title: Construction of MOSFET Logic Gates (Part I)

Introduction:

We learned how Construction of MOSFET Logic Gates works. It signifies that the MOSFET can be powered by the general-purpose logic IC's output voltage (4 to 5 V). The MOSFET cannot be powered if the general-purpose logic IC does not have enough output current capabilities. With a simple example of a Diode-Resistor Logic (DRL) AND gate and a Diode-Transistor Logic (DTL) NAND gate, simple digital logic gates can be built by combining transistors, diodes, and resistors.

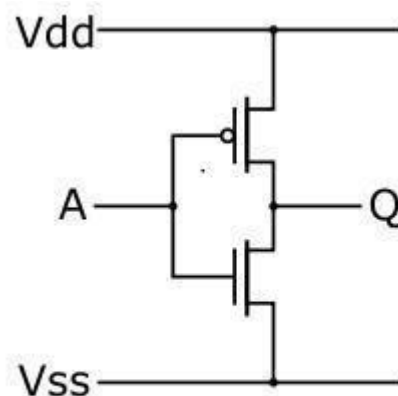
Theory and Methodology:

MOSFET:

MAWS-feht is the correct pronunciation. Metal-oxide semiconductor field-effect transistor is an acronym. These are utilized in a variety of situations when voltage conversion is required. To create CPU, memory, and AGP voltages, for example, on your motherboard. Mosfets are typically employed in groups of two. Three-phase power is indicated by the presence of six mosfets around the CPU socket.

CMOS:

CMOS (complementary metal–oxide–semiconductor) is an integrated circuit fabrication method. Microprocessors, microcontrollers, static RAM, and other digital logic circuits all utilise CMOS technology. CMOS technology is also used for several analog circuits such as image sensors (CMOS sensor), data converters, and highly integrated transceivers for many types of communication. In 1963, Frank Wanlass received a patent on CMOS (US patent 3,356,858). Complementary-symmetry metal–oxide–semiconductor is another name for CMOS (or COS-MOS). The term "complementary-symmetry" refers to how CMOS logic functions are often implemented using complementary and symmetrical pairings of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs).



CMOS inverter ([NOT logic gate](#))

High noise immunity and low static power consumption are two significant properties of CMOS electronics. Because one of the pair's transistors is permanently off, the series combination only drains substantial power while transitioning between on and off states. As a result, CMOS devices produce less waste heat than other types of logic, such as transistor–transistor logic (TTL) or NMOS logic, which typically have some standing current even when not in use. In addition, CMOS enables for a high density of logic functions on a single chip. It was primarily for this reason that CMOS became the most widely utilized technology for VLSI chips.

Here Some the advantages of CMOS over TTL are:

1. Because MOSFETs are voltage-controlled rather than current-controlled semiconductors, CMOS gate inputs draw significantly less current than TTL inputs.
2. CMOS gates can operate over a far larger range of voltages than TTL gates: typically 3 to 15 volts against 4.75 to 5.25 volts for TTL gates.
3. CMOS transistors are smaller than NMOS transistors and have lower power dissipation.

NMOS Inverter with Ohmic/ Resistive Load:

In a perfect scenario, when HIGH (+5V) is applied to the input, the NMOS transistor is turned on and current flows from V_{dd} to ground, resulting in an output voltage of 0V. Similarly, if the input voltage is LOW (0V), the NMOS remains in the OFF state. As a result, there is no path for the current from V_{dd} to reach Earth. The voltage at the output is +5V.

NMOS Inverter with NMOS Enhancement Transistor load:

One downside of using an ohmic load in NMOS logic circuits is that there remains static power dissipation owing to the resistor even when the NMOS is turned off. As a load, an enhancement-type NMOS is a preferable choice. They are "normally-off" devices that must be biased on by applying the correct polarity voltage between gate and drain. As a result, static power usage is reduced.

CMOS Logic:

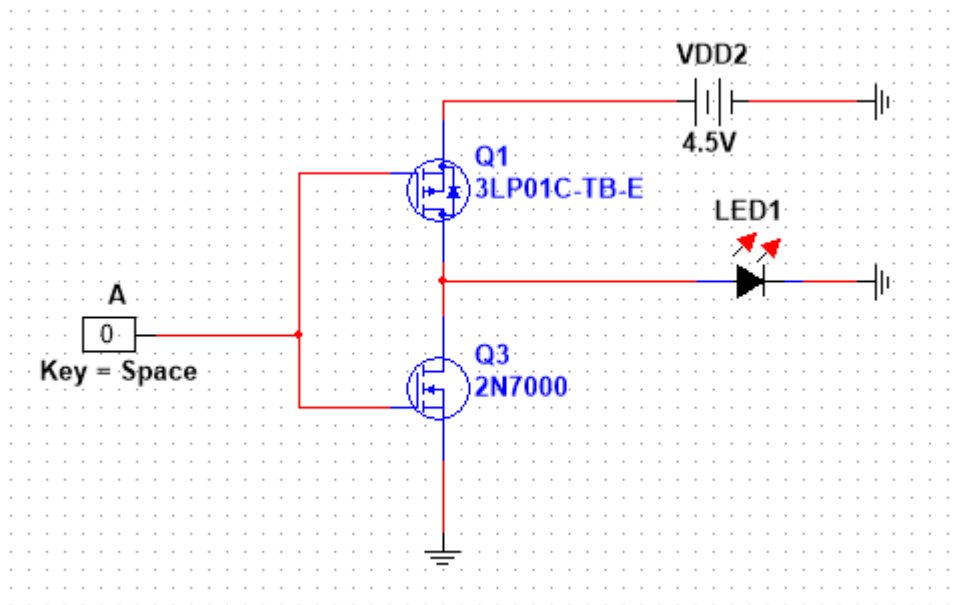
CMOS transistors are smaller than NMOS transistors and have lower power dissipation. Thus they became the obvious choice of replacing NMOS transistors at the integrating circuit level design in all applications. CMOS consists of one p-channel MOSFET or PMOS and one NMOS. The two MOSFETs have been engineered to have similar properties. Thus, they are complementary to each other. When OFF, their resistance is effectively infinite; when ON, their channel resistance is quite low (around 200 Ω). Since the gate is essentially an open circuit it draws no current and the output voltage will be equal to either ground or to the power supply voltage, depending on which transistor is conducting.

CMOS Inverter:

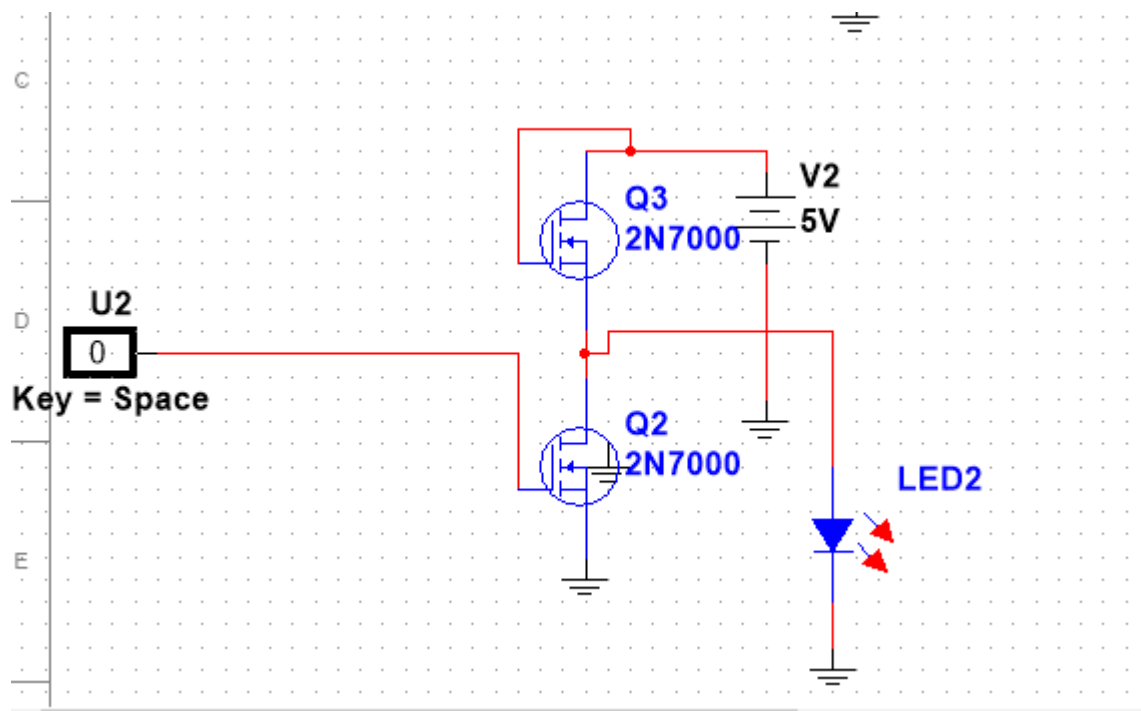
One p-channel MOSFET or PMOS and one NMOS make up CMOS. The two MOSFETs are made to work together. The N-channel MOSFET is unbiased when the input is grounded (logic 0), and so has no channel enhancement inside itself. Because it is an open circuit, the output line is isolated from ground. The P-channel MOSFET, on the other hand, is forward biased and hence has a channel enhanced within itself. This channel connects the output line to the +V supply and has a resistance of roughly 200 ohms. This raises the output voltage to +V. (logic 1). The P-channel MOSFET is off and the N-channel MOSFET is on when input A is at +V (logic 1), pulling the output down to ground (logic 0). As a result, this circuit executes logic inversion correctly while also providing active pull-up and pull-down, depending on the output state.

Diagram & Simulation :

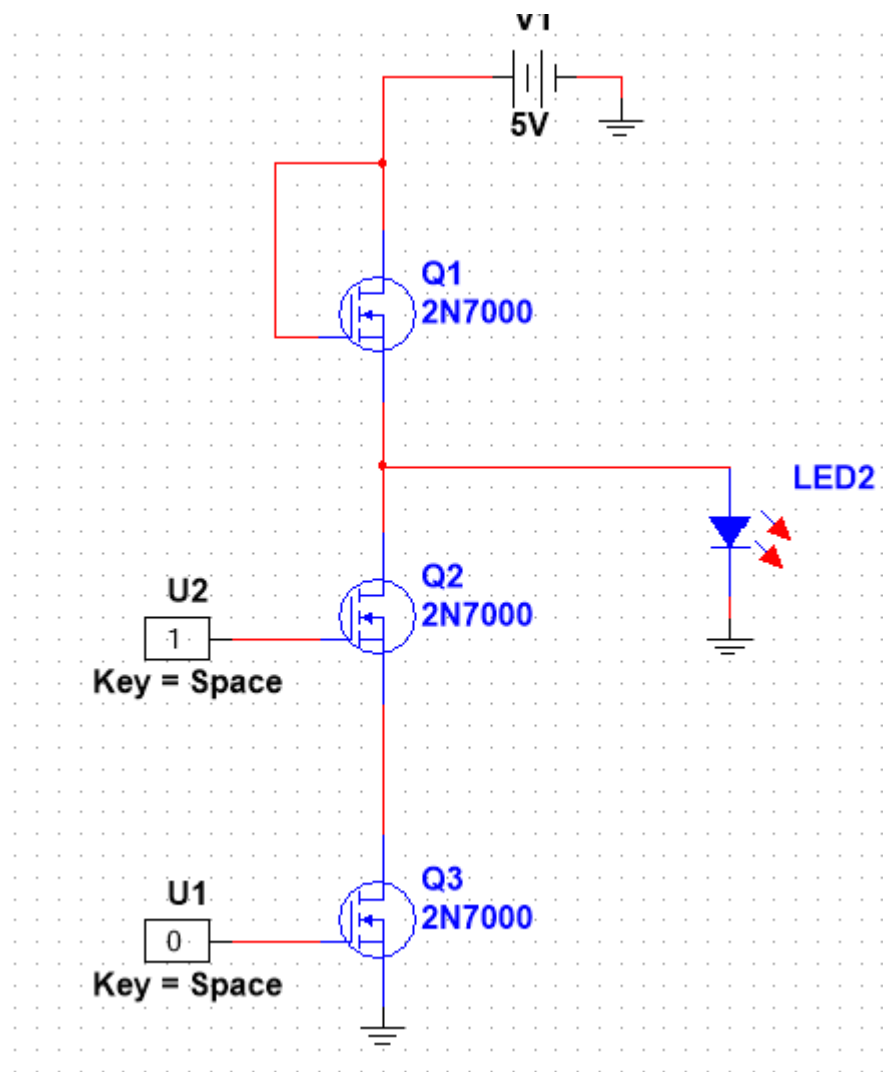
cmos inverter



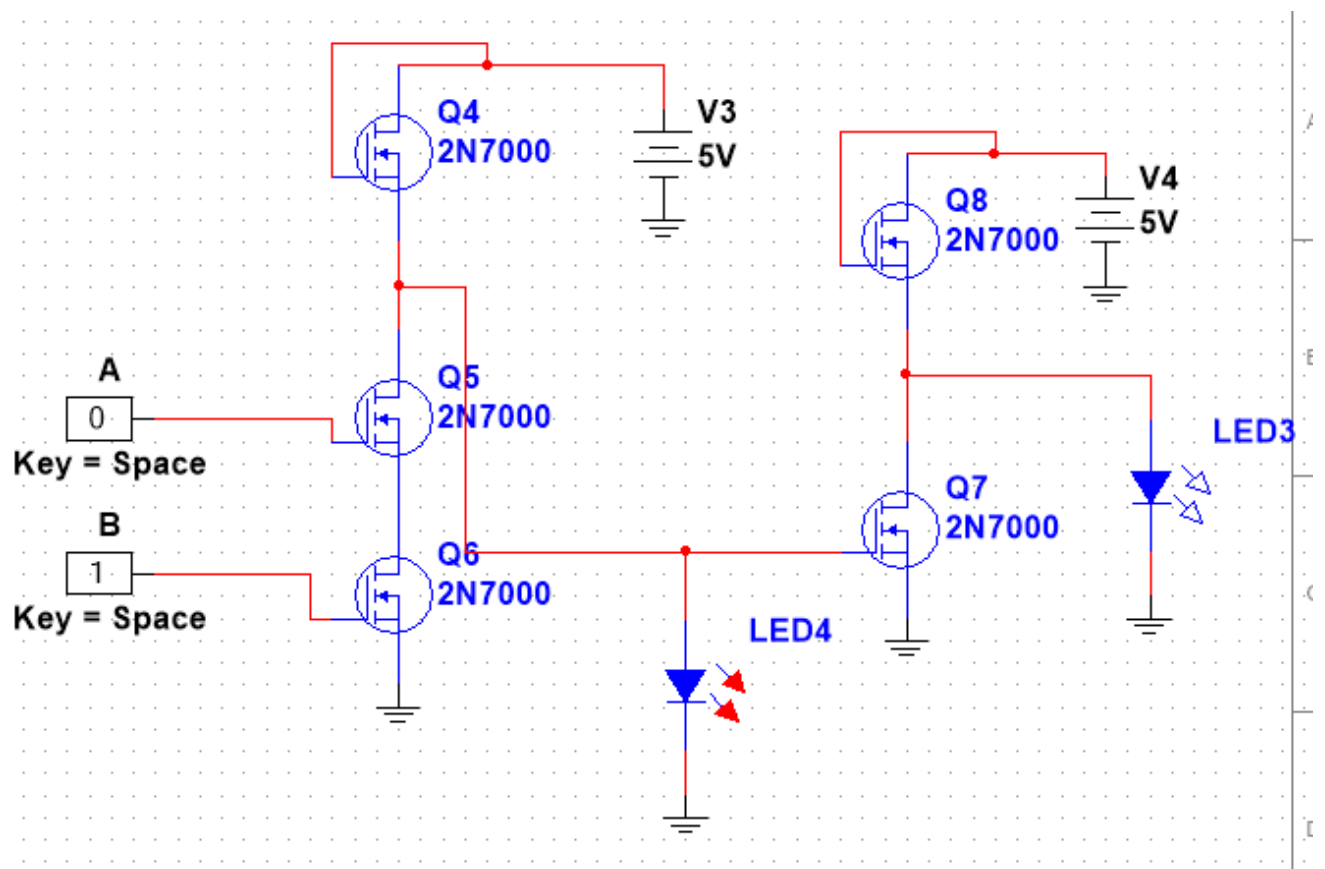
nmos inverter



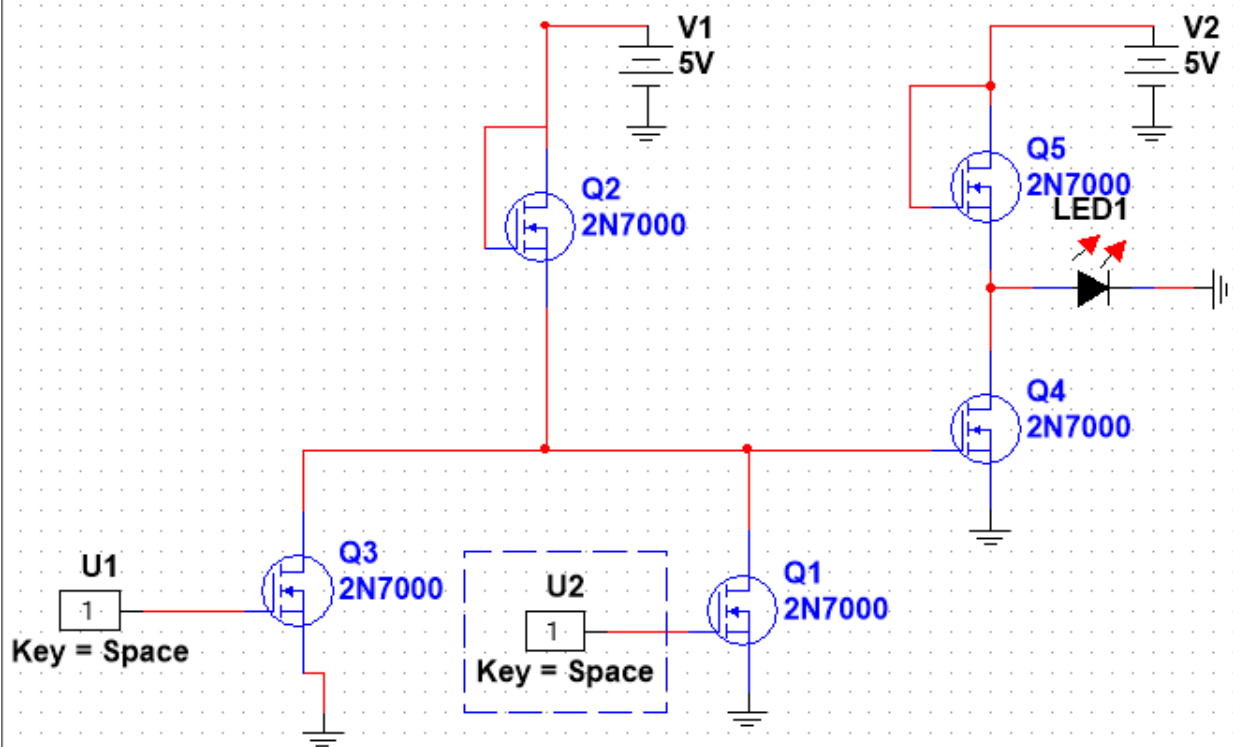
nmos nand



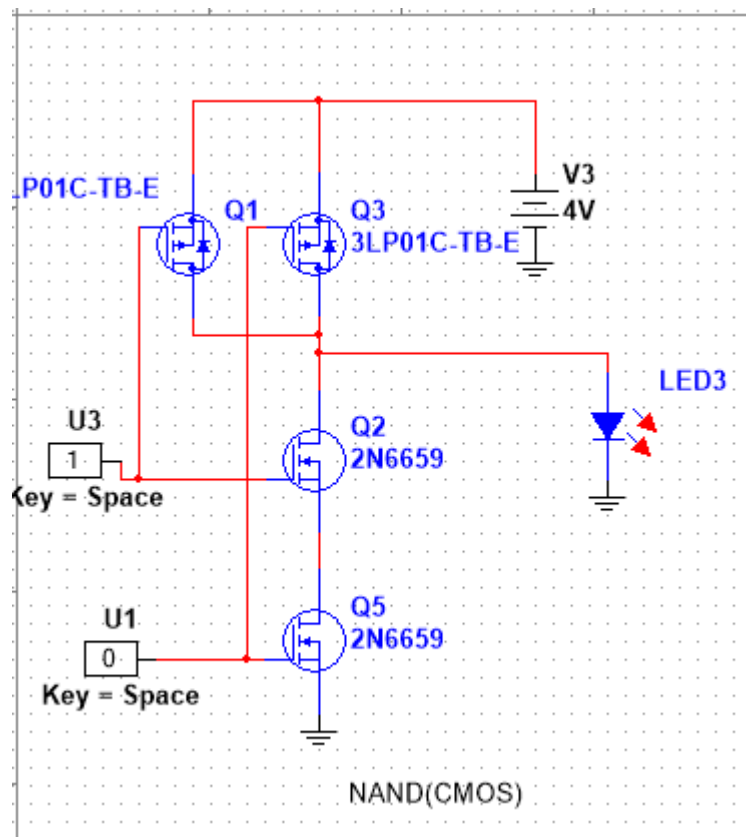
nmos and



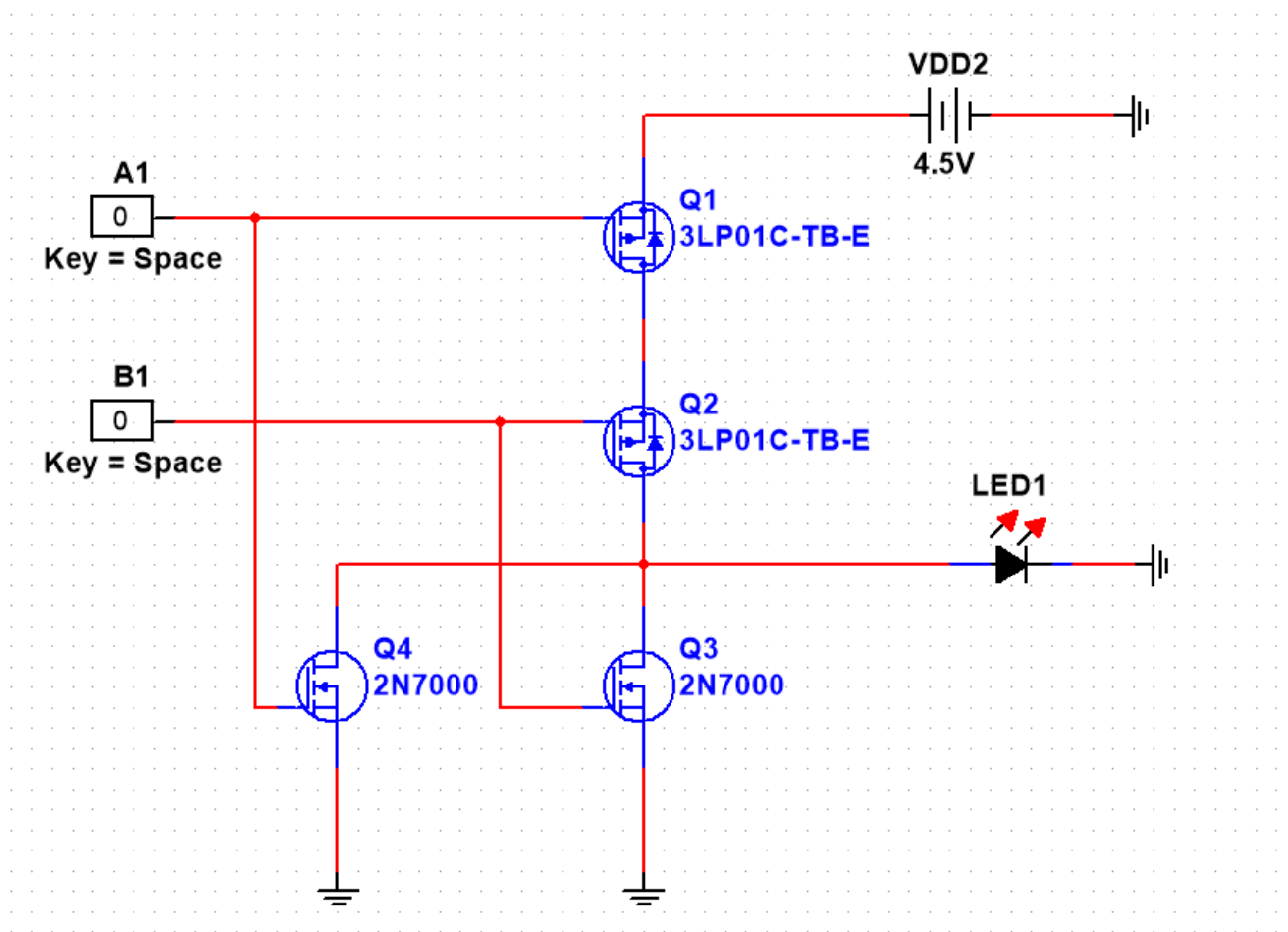
nor and or and gate nmos



cmos nand



cmos nor



Results: Result was as expected no error was being faced. The truth table and circuit gave exact results. The truth table result and circuit result matched while simulating.

Discussion: In this experiment, we have used NI Multisim version -14.2 software for the Simulations. We faced some problems while finding the components in the software that's why it took a much extra time. The overall outcome was excellent for finding the answer using the application, and implementing the circuit was quite difficult for beginners. At first, we had to learn about **Construction of MOSFET Logic Gates(mosfet,cmosfet,nmosfet)**. After that, we can get ready to work with Multisim Software. Then, we successfully assembled all of the components on the Multisim bread board without any faults. Successfully we have confirmed to build the connection between the circuit wires without any problem. At last our Truth table was verified by simulations result and they also matched with each other.

Reference:

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3. https://pages.jh.edu/aandreo1/216/Archives/2014/Handouts/POP_Ch3-4.pdf
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